High Speed, 3.3 V/5 V Quad 2:1 Mux/Demux (4-Bit, 1 of 2) Bus Switch

ADG3257

FEATURES

100 ps propagation delay through the switch
2 Ω switches connect inputs to outputs
Data rates up to 933 Mbps
Single 3.3 V/5 V supply operation
Level translation operation
Ultralow quiescent supply current (1 nA typical)
3.5 ns switching
Switches remain in the off state when power is off
Standard 3257 type pinout

APPLICATIONS

Bus switching
Bus isolation
Level translation
Memory switching/interleaving

GENERAL DESCRIPTION

The ADG3257 is a CMOS bus switch comprised of four 2:1 multiplexers/demultiplexers with high impedance outputs. The device is manufactured on a CMOS process. This provides low power dissipation yet high switching speed and very low on resistance, allowing the inputs to be connected to the outputs without adding propagation delay or generating additional ground bounce noise.

The ADG3257 operates from a single 3.3 V/5 V supply. The control logic for each switch is shown in Table 1. These switches are bidirectional when on. In the off state, signal levels are blocked up to the supplies. When the power supply is off, the switches remain in the off state, isolating Port A and Port B.

This bus switch is suited to both switching and level translation applications. It can be used in applications requiring level translation from 3.3 V to 2.5 V when powered from 3.3 V. Additionally, with a diode connected in series with 5 V V_{DD}, the ADG3257 may also be used in applications requiring 5 V to 3.3 V level translation.

Table 1. Truth Table

$\overline{BE}$	S	Function
H	X	Disable
L	L	$A = B_1$
L	H	$A = B_2$

FUNCTIONAL BLOCK DIAGRAM

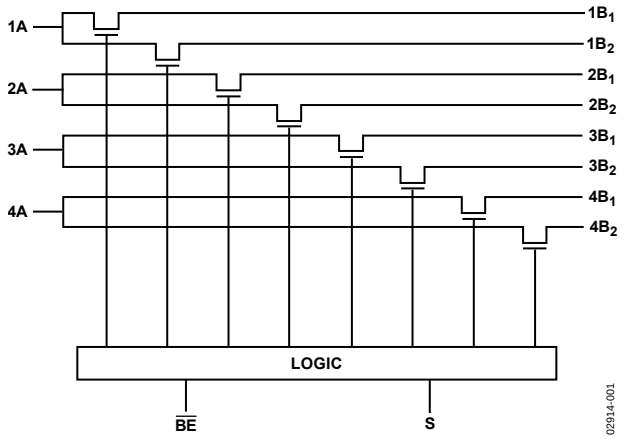

Figure 1.

PRODUCT HIGHLIGHTS

1. 0.1 ns propagation delay through switch.
2. 2 Ω switches connect inputs to outputs.
3. Bidirectional operation.
4. Ultralow power dissipation.
5. 16-lead QSOP package.

Rev. E

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SPECIFICATIONS

V_{CC} = 5.0 V ± 10%, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

			B Version			
Parameter[1]	**Symbol**	**Conditions[2]**	**Min**	**Typ[3]**	**Max**	**Unit**
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}		2.4			V
Input Low Voltage	V_{INL}		−0.3		+0.8	V
Input Leakage Current	I_I	$0 \le V_{IN} \le 5.5$ V		±0.01	±1	µA
Off State Leakage Current	I_{OZ}	$0 \le A, B \le V_{CC}$		±0.01	±1	µA
On State Leakage Current	I_{OZ}	$0 \le A, B \le V_{CC}$		±0.01	±1	µA
Maximum Pass Voltage[4]	V_P	$V_{IN} = V_{CC} = 5$ V, $I_O = -5$ µA	3.9	4.2	4.4	V
CAPACITANCE[4]						
A Port Off Capacitance	C_A OFF	f = 1 MHz		7		pF
B Port Off Capacitance	C_B OFF	f = 1 MHz		5		pF
A, B Port On Capacitance	C_A, C_B ON	f = 1 MHz		11		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		4		pF
SWITCHING CHARACTERISTICS[4]						
Propagation Delay A to B or B to A, t_{PD}	t_{PHL}, t_{PLH}[5]	$V_A = 0$ V, $C_L = 50$ pF			0.10	ns
Propagation Delay Matching[6]		$V_A = 0$ V, $C_L = 50$ pF		0.0075	0.035	ns
Bus Enable Time $\overline{BE}$ to A or B	t_{PZH}, t_{PZL}	$C_L = 50$ pF, $R_L = 500$ Ω	1	5	7.5	ns
Bus Disable Time $\overline{BE}$ to A or B	t_{PHZ}, t_{PLZ}	$C_L = 50$ pF, $R_L = 500$ Ω	1	3.5	7	ns
Bus Select Time S to A or B						
Enable	t_{SEL_EN}	$C_L = 50$ pF, $R_L = 500$ Ω		8	12	ns
Disable	t_{SEL_DIS}	$C_L = 50$ pF, $R_L = 500$ Ω		5	8	ns
Maximum Data Rate		$V_A = 2$ V p-p		933		Mbps
DIGITAL SWITCH						
On Resistance	R_{ON}	$V_A = 0$ V				
		$I_O = 48$ mA, 15 mA, 8 mA, $T_A = 25$°C		2	4	Ω
		$I_O = 48$ mA, 15 mA, 8 mA			5	Ω
		$V_A = 2.4$ V				
		$I_O = 48$ mA, 15 mA, 8 mA, $T_A = 25$°C		3	6	Ω
		$I_O = 48$ mA, 15 mA, 8 mA			7	Ω
On-Resistance Matching	ΔR_{ON}	$V_A = 0$ V, $I_O = 48$ mA, 15 mA, 8 mA		0.15		Ω
POWER REQUIREMENTS						
V_{CC}			3.0		5.5	V
Quiescent Power Supply Current	I_{CC}	Digital inputs = 0 V or V_{CC}		0.001	1	µA
Increase in I_{CC} per Input[4, 7]	ΔI_{CC}	$V_{CC} = 5.5$ V, one input at 3.0 V; others at V_{CC} or GND			200	µA

[1] Temperature range is: Version B: −40°C to +85°C.
[2] See Test Circuits section.
[3] All typical values are at T_A = 25°C, unless otherwise noted.
[4] Guaranteed by design, not subject to production test.
[5] The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Because the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
[6] Propagation delay matching between channels is calculated from on-resistance matching of worst-case channel combinations and load capacitance.
[7] This current applies to the control pins only and represents the current required to switch internal capacitance at the specified frequency. The A and B ports contribute no significant ac or dc currents as they transition.

V_{CC} = 3.3 V ± 10%, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	Symbol	Conditions[2]	B Version			Unit
			Min	Typ[3]	Max	
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}		−0.3		+0.8	V
Input Leakage Current	I_I	0 ≤ V_{IN} ≤ 3.6 V		±0.01	±1	µA
Off State Leakage Current	I_{OZ}	0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
On State Leakage Current	I_{OZ}	0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
Maximum Pass Voltage[4]	V_P	V_{IN} = V_{CC} = 3.3 V, I_O = −5 µA	2.3	2.6	2.8	V
CAPACITANCE[4]						
A Port Off Capacitance	C_A OFF	f = 1 MHz		7		pF
B Port Off Capacitance	C_B OFF	f = 1 MHz		5		pF
A, B Port On Capacitance	C_A, C_B ON	f = 1 MHz		11		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		4		pF
SWITCHING CHARACTERISTICS[4]						
Propagation Delay A to B or B to A, t_{PD}	t_{PHL}, t_{PLH}[5]	V_A = 0 V, C_L = 50 pF			0.10	ns
Propagation Delay Matching[6]		V_A = 0 V, C_L = 50 pF		0.01	0.04	ns
Bus Enable Time $\overline{BE}$ to A or B	t_{PZH}, t_{PZL}	C_L = 50 pF, R_L = 500 Ω	1	5.5	9	ns
Bus Disable Time $\overline{BE}$ to A or B	t_{PHZ}, t_{PLZ}	C_L = 50 pF, R_L = 500 Ω	1	4.5	8.5	ns
Bus Select Time S to A or B						
Enable	t_{SEL_EN}	C_L = 50 pF, R_L = 500 Ω		8	12	ns
Disable	t_{SEL_DIS}	C_L = 50 pF, R_L = 500 Ω		6	9	ns
Maximum Data Rate		V_A = 2 V p-p		933		Mbps
DIGITAL SWITCH						
On Resistance	R_{ON}	V_A = 0 V, I_O = 15 mA, 8 mA, T_A = 25°C		2	4	Ω
		V_A= 0 V, I_o = 15 mA, 8 mA			5	Ω
		V_A = 1 V, I_O = 15 mA, 8 mA, T_A = 25°C		4	7	Ω
		V_A= 1 V, I_o = 15 mA, 8 mA			8	Ω
On-Resistance Matching	ΔR_{ON}	V_A = 0 V, I_O = 15 mA, 8 mA		0.2		Ω
POWER REQUIREMENTS						
V_{CC}			3.0		5.5	V
Quiescent Power Supply Current	I_{CC}	Digital inputs = 0 V or V_{CC}		0.001	1	µA
Increase in I_{CC} per Input[4, 7]	ΔI_{CC}	V_{CC} = 3.3 V, one input at 3.0 V; others at V_{CC} or GND			200	µA

[1] Temperature range is: Version B: −40°C to +85°C.
[2] See Test Circuits section.
[3] All typical values are at T_A = 25°C, unless otherwise noted.
[4] Guaranteed by design, not subject to production test.
[5] The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Because the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
[6] Propagation delay matching between channels is calculated from on-resistance matching of worst-case channel combinations and load capacitance.
[7] This current applies to the control pins only and represents the current required to switch internal capacitance at the specified frequency. The A and B ports contribute no significant ac or dc currents as they transition.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{CC} to GND	−0.3 V to +6 V
Digital Inputs to GND	−0.3 V to +6 V
DC Input Voltage	−0.3 V to +6 V
DC Output Current	100 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
QSOP Package	
θ_{JA} Thermal Impedance	149.97°C/W
Lead Soldering	
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	220°C
Soldering (Pb-Free)	
Reflow, Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

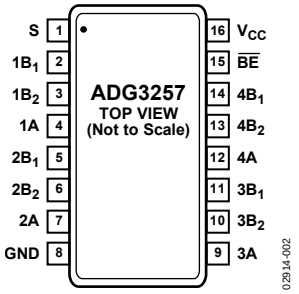

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S	Port Select.
2, 3, 5, 6, 10, 11, 13, 14	$1B_1$, $1B_2$, $2B_1$, $2B_2$, $3B_2$, $3B_1$, $4B_2$, $4B_1$	Port B, Inputs or Outputs.
4, 7, 9, 12	1A, 2A, 3A, 4A	Port A, Inputs or Outputs.
8	GND	Negative Power Supply.
15	$\overline{BE}$	Output Enable (Active Low).
16	V_{CC}	Positive Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

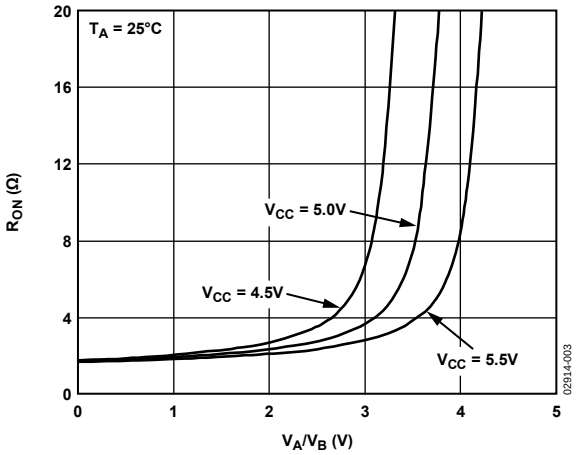

Figure 3. On Resistance vs. Input Voltage

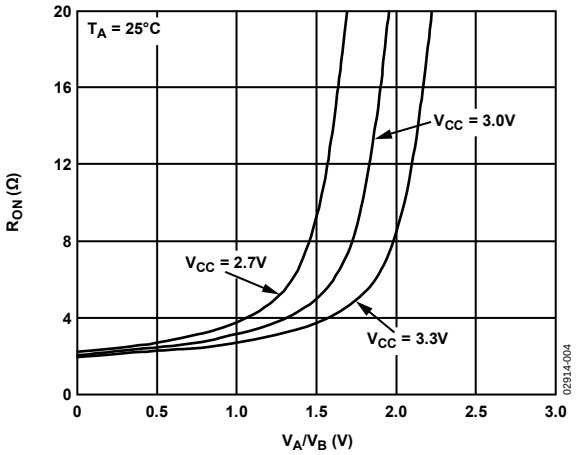

Figure 4. On Resistance vs. Input Voltage

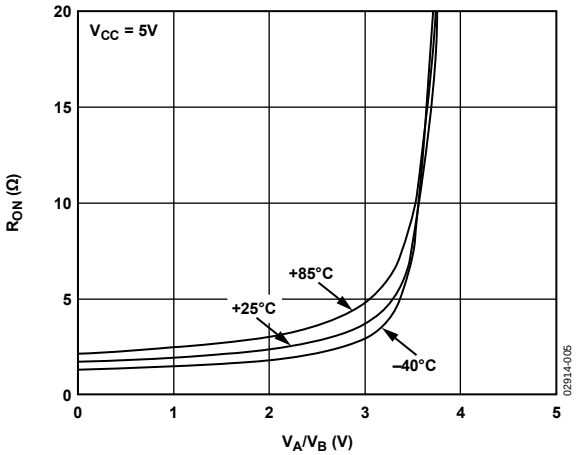

Figure 5. On Resistance vs. Input Voltage for Different Temperatures

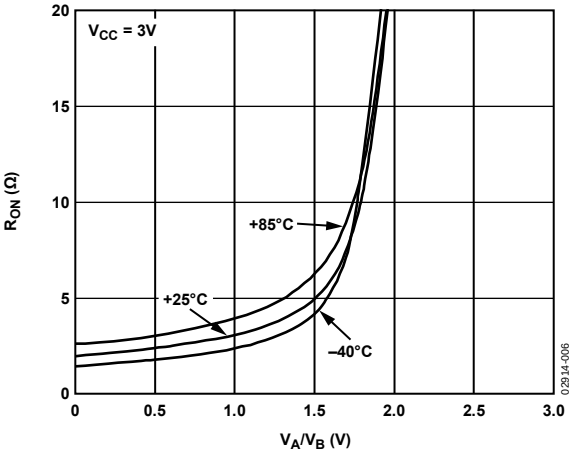

Figure 6. On Resistance vs. Input Voltage for Different Temperatures

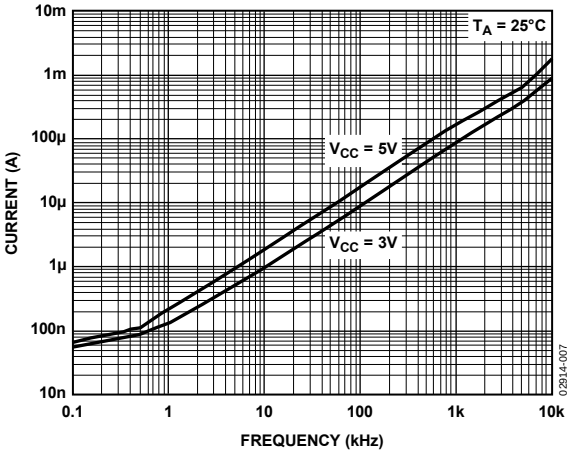

Figure 7. I_{CC} vs. Enable Frequency

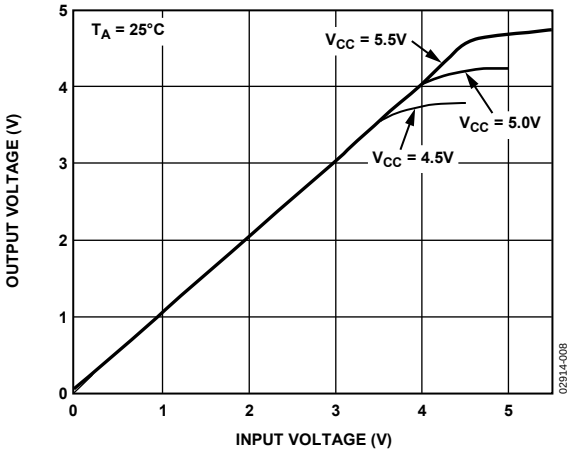

Figure 8. Maximum Pass Voltage

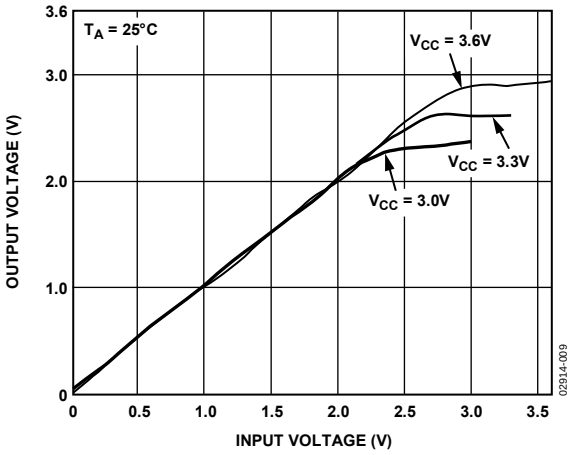

Figure 9. Maximum Pass Voltage

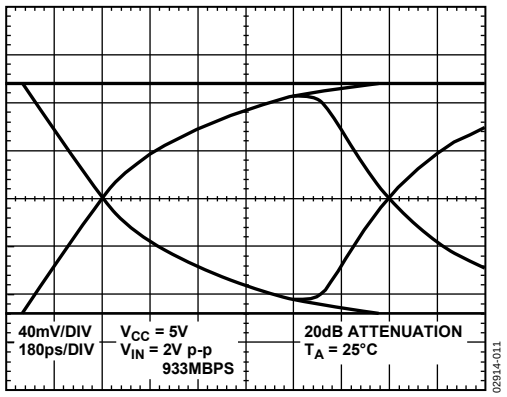

Figure 11. 933 Mbps Eye Diagram

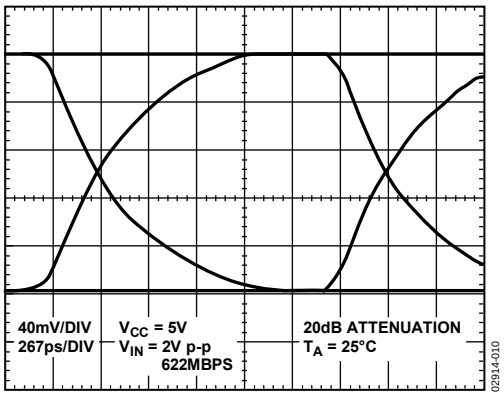

Figure 10. 622 Mbps Eye Diagram

TEST CIRCUITS

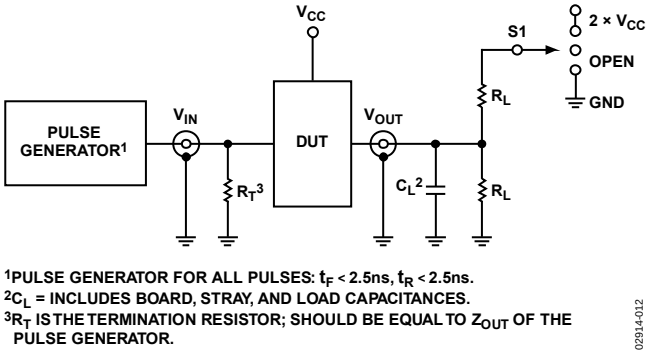

Figure 12. Load Circuit

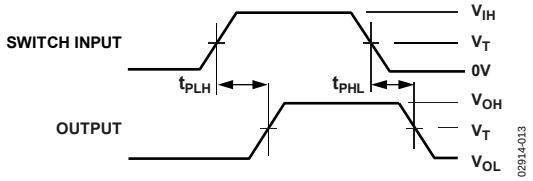

Figure 13. Propagation Delay

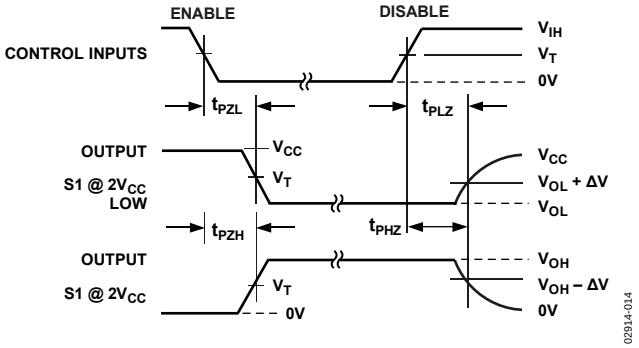

Figure 14. Select, Enable, and Disable Times

Table 6. Switch S1 Condition

Test	S1
t_{PLH}, t_{PHL}	Open
t_{PLZ}, t_{PZL}	2 × V_{CC}
t_{PHZ}, t_{PZH}	GND
t_{SEL}	Open

Table 7. Test Conditions

Symbol	V_{CC} = 5 V ± 10%	V_{CC} = 3.3 V ± 10%	Unit
R_L	500	500	Ω
ΔV	300	300	mV
C_L	50	50	pF

APPLICATIONS INFORMATION

MIXED VOLTAGE OPERATION, LEVEL TRANSLATION

Bus switches can be used to provide a solution for mixed voltage systems where interfacing bidirectionally between 5 V and 3.3 V devices is required. To interface between 5 V and 3.3 V buses, an external diode is placed in series with the 5 V power supply as shown in Figure 15.

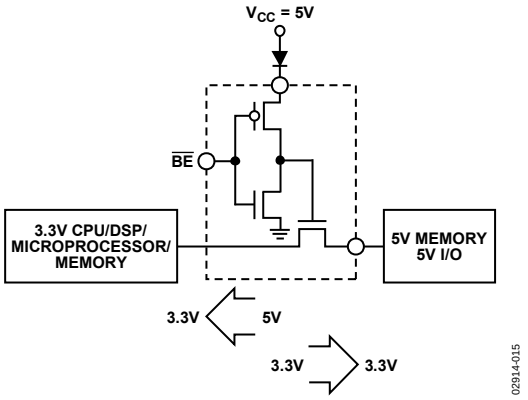

Figure 15. Level Translation Between 5 V and 3.3 V Devices

The diode drops the internal gate voltage down to 4.3 V. The bus switch limits the voltage present on the output to

V_{CC} – *External Diode Drop* = V_{TH}

Therefore, assuming a diode drop of 0.7 V and a V_{TH} of 1 V, the output voltage is limited to 3.3 V with a logic high.

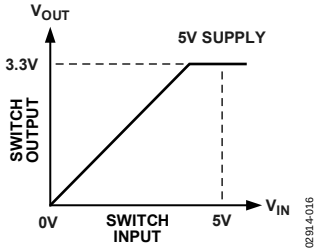

Figure 16. Input Voltage to Output Voltage

Similarly, the device could be used to translate bidirectionally between 3.3 V to 2.5 V systems. In this case, there is no need for an external diode. The internal V_{TH} drop is 1 V, so with a V_{CC} = 3.3 V the bus switch limits the output voltage to

V_{CC} – 1 V = 2.3 V

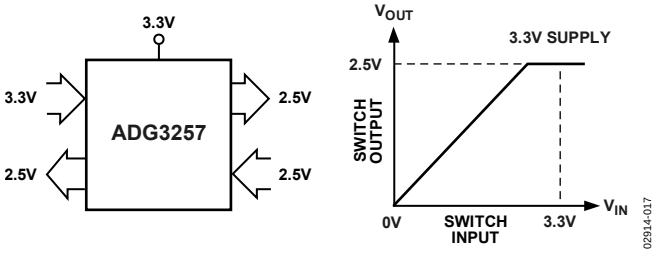

Figure 17. 3.3 V to 2.5 V Level Translation Using the ADG3257 Bus Switch

MEMORY SWITCHING

This quad bus switch may be used to allow switching between different memory banks, thus allowing additional memory and decreasing capacitive loading. Figure 18 illustrates the ADG3257 in such an application.

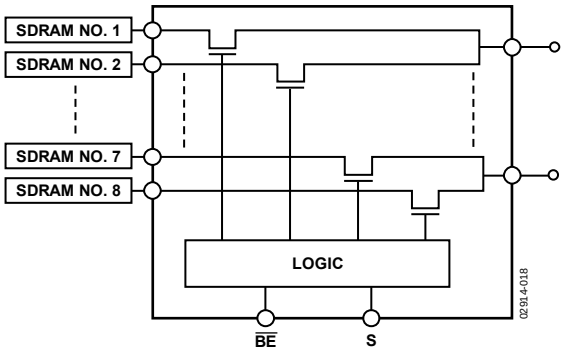

Figure 18. Allows Additional Memory Modules Without Added Drive or Delay

OUTLINE DIMENSIONS

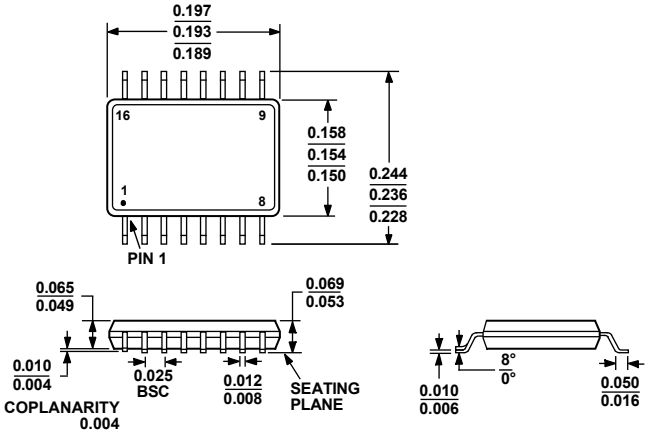

Figure 19. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG3257BRQ	–40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG3257BRQ-REEL	–40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG3257BRQ-REEL7	–40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG3257BRQZ[1]	–40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG3257BRQZ-REEL[1]	–40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG3257BRQZ-REEL7[1]	–40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16

[1] Z = RoHS Compliant Part.

NOTES

D02914-0-3/08(E)